Exp. Mail EV005526031US

10082984.022502

S P E C I F I C A T I O N

BE IT KNOWN THAT WE, YUKINOBU KONISHI, AKIO NAKAYAMA and KAZUHIRO KOBAYASHI, all residing at c/o ADVANCED DISPLAY INC., 997, Miyoshi, Nishigoshi-machi, Kikuchi-gun, Kumamoto 861-1198 Japan, subjects of Japan, have invented certain new and useful improvements in

LIQUID CRYSTAL DISPLAY

of which the following is a specification:-

LIQUID CRYSTAL DISPLAY

FIELD OF THE INVENTION

The present invention relates to a liquid crystal display, and more particularly, relates to an active-matrix liquid crystal display in which thin film transistors are employed as switching devices.

BACKGROUND OF THE INVENTION

In liquid crystal displays (hereinafter LCDs), liquid crystal material is sandwiched between a pair of substrates. Fig. 5 is an enlarged plain view of one of the substrates. On the substrate, pixel electrodes 15 are arranged in a matrix like manner of rows and columns as shown in Fig. 5. Furthermore, a switching device is provided for each pixel electrode to selectively apply voltage to the pixel electrode. Usually, a thin film transistor (hereinafter TFT) 17 is used as the switching device. Therefore, this substrate is called "a TFT array substrate". On the TFT array substrate, gate lines 2 and source lines 9 are provided to supply electric signals to respective TFTs 17. When the TFT turns "ON" by applying a signal to the gate line 2, voltage on the source line 9 is written into the pixel electrode 15. The other substrate, which is often called "a counter substrate", has a counter electrode formed thereon. Accordingly, liquid crystal interposed between the counter electrode and the pixel electrode is driven by potential difference between the electrodes, thereby obtaining any required display.

In Fig. 4, a plain view of the whole TFT array substrates is shown. The pixel electrodes 15 and the TFTs 17 are provided in a display area 22, and terminal forming regions 20, 21, in which terminals

are formed, are provided around the display area 22. In the regions 20, 21, source terminals 18 and gate terminals 19 are formed respectively. The source terminal 18 is connected to the source line 9 in the display area 22. The gate terminal 19 is connected to the gate line 2 in the display area 22.

In order to protect the TFTs 17 from destruction by, for example, electrostatic discharge during fabrication process, the source terminals 18 and the gate terminal 19 are connected to a short-circuit ring 23. At the final stage of the fabrication process, the short-circuit ring 23 is removed by cutting off the edge of the TFT array substrate. Thereafter, wirings from external signal source are attached to the source terminals 18 and the gate terminals 19, therefore fabrication of LCD is completed.

Hereinafter, fabrication process of the TFT array substrate is described with referring to Figs. 6, 7 and 8. Figs. 6 and 7 are cross sectional view of the TFT array substrate showing a TFT and a source terminal formed thereon, and describing fabrication steps thereof. Fig. 8 is a magnified view of the source terminal 18 in Fig. 7(c). Fig. 8(a) is a plain view of the source terminal 18, and Fig. 8(b) is a cross sectional view taken along line B-B in Fig. 8(a).

In the figure, a transparent insulating substrate 1, such as a glass substrate, is shown. Of course, a simply insulating substrate is also applicable. On the substrate 1, a gate line 2 is formed. The gate line 2 is made from a metal film such as a film of Al or Cr. On the gate line 2 and covering the substrate 1, a gate insulating layer 4 is formed. The gate insulating layer 4 is made of silicon nitride.

Above the gate line 2 and interposing the gate insulating layer

4, a semiconductor layer 5 is formed. The semiconductor layer 5 is made from, for example, a film of amorphous silicon. On the semiconductor layer 5, a contact layer 6 is formed. The contact layer 6 is made from a film of n+ amorphous silicon. On the contact layer 6, a source electrode 7 and a drain electrode 8 are formed. With the source electrode 7 and the drain electrode 8, a source line 9 is formed at the same time. By etching the contact layer 6 partly, a channel 10 of the TFT is formed. Not to expose the TFT 17, a passivation film 11 is formed. The passivation film 11 is made of silicon nitride.

On the drain electrode 8 and through the passivation film 11, a contact hole 12 is formed for connecting the drain electrode 8 with a pixel electrode 15. On the source line 9 and through the passivation film 11, a contact hole 13 is formed for connecting the source line 9 with a terminal electrode 16. The pixel electrode 15 is made from a film of indium tin oxide (ITO). With the pixel electrode 15, the terminal electrode 16 is formed from the same ITO film at the same time.

Hereinafter, fabrication process of the TFT array substrate is described more in detail with referring to Figs. 6, 7 and 8.

First of all, a metal film, such as a film of Cr or Al, is formed on an insulating substrate 1 by sputtering method. Then, the film is patterned using photo resist through photolithography to form a gate line 2 (Fig. 6(a)).

Thereafter, a silicon nitride film as a gate insulating layer 4 is deposited onto the substrate 1 with the gate line 2, by a plasma CVD method (Fig. 6(b)). Further, an amorphous silicon film is formed thereon, and successively, a n+ amorphous silicon film in which impurities are doped is formed. Then, the amorphous silicon film and

the n+ amorphous silicon film are simultaneously patterned using photo resist through photolithography to form a semiconductor layer 5 and the contact layer 6 of TFT above the gate line 2 (Fig. 6(c)).

Afterwards, a metal film such as Cr film or Al film is formed by a method such as sputtering. Then, the film is patterned using photo resist through photolithography to form a source electrode 7, drain electrode 8 and source line 9. Thereafter, the n+ amorphous silicon (contact layer 6) is partly etched, that is, an area on which neither the source electrode 7 nor the drain electrode 8 is formed is etched through dry-etching process, so that the channel 10 is formed (Fig. 7(a)).

Then, to provide protection for TFTs, a silicon nitride film as a passivation film 11 is deposited by a method such as plasma CVD. Thereafter, through dry-etching process using photo resist by photolithography, contact holes 12 and 13 are formed (Fig. 7(b)). As described above, the contact hole 12 is for connecting the drain electrode 8 with a pixel electrode 15, and the contact hole 13 is for connecting the source line 9 with a terminal electrode 16.

Afterwards, a transparent conductive film such as an ITO film is formed by a method such as sputtering. Then, the film is patterned using photo resist through photolithography, so that the pixel electrode 15 and the terminal electrode 16 are formed simultaneously. As described above, the terminal electrode 16 is for connection to external signal source.

For the TFT array substrate thus fabricated, an enlarged view around the source terminal 18 is shown in Fig. 8. As described above, the terminal electrode 16 is positioned as the uppermost layer of the source terminal 18 for external connection. The terminal electrode 16

is also connected to the source line 9 via the contact hole 13 and an end of the source line 9 is connected to the source electrode 7 of the TFT 17, that is, internal connection. In the meantime, the other end of the source line 9 is connected to the short-circuit ring 23 (see Fig. 4).

At the final stage of the fabrication, the edge of the TFT array substrate is cut off and chamfered off along the line 24 to remove the short-circuit ring 23. However, especially when the edge of the substrate is chamfered, the source line 9 can be peeled off. The peeled metal pieces may contact each other to electrically connect the adjacent terminals, so that a problem of short-circuit between adjacent lines can be caused. Moreover, in case where the cutting line 24 is designed to be closer to the terminal electrode, or in case where the cutting line 24 is accidentally closed to the terminal electrode due to inaccuracy of manufacturing equipment, the peeled metal piece may contact with the terminal electrode of the adjacent terminal to cause a problem of short-circuit between adjacent lines.

As is already described above and as shown in Fig. 8, a single metallic layer is arranged below the terminal electrode 16 at the source terminal 18, in the conventional TFT array substrate. Namely, both the display area side (the right side in Fig. 8) and the short-circuit ring side (the left side in Fig. 8), the same metallic layer, that is, the source line 9 is arranged below the terminal electrode 16.

In this conventional structure, when the substrate is chamfered along the cutting line 24, the source line 9 at the edge is easily exfoliated to appear as a peeled metal piece. Therefore, since the peeled metal pieces easily contact each other to cause short-circuit between neighboring terminals, short-circuit between neighboring lines

frequently occurs. Furthermore, the peeled metal piece easily contacts with the terminal electrode of the neighboring terminal and causes short-circuit between neighboring lines.

SUMMARY OF THE INVENTION

The object of the present invention is to solve the above problems, and to obtain liquid crystal display of high reliability by preventing exfoliation of the metallic film in cutting and chamfering process of the substrate.

In a liquid crystal display according to the present invention, liquid crystal is interposed between substrates. One of the substrates is provided with a display area and a terminal forming area. In the display area, a pixel electrode, a switching element connected to the pixel electrode, a gate line connected to the switching element and a source line connected to the switching element are formed. In the terminal forming area, a terminal electrode for connecting the gate line or source line to external signal source is formed. Moreover, around the terminal forming area, a first metallic line and a second metallic line are extended below the terminal electrode. The first metallic line and the second metallic line are connected to the terminal electrode via respective contact holes. The first metallic line and the second metallic line are in different layers interposing an insulating layer therebetween.

Moreover, either the first metallic line or the second metallic line is in the same layer as that for the gate line and the other metallic line is in the same layer as that for the source line.

Furthermore, either the first metallic line or the second metallic line is connected to the source line and the other metallic line is

in a lower layer as that for the metallic line connected to the source line.

Elsewhere, either the first metallic line or the second metallic line is connected to the gate line and the other metallic line is in a lower layer as that for the metallic line connected to the gate line.

According to the present invention, since the metallic line around the cutting line is arranged in a lower layer than that in the conventional liquid crystal display, scraping of the metallic line is suppressed. Therefore, exfoliation of the metallic film is reduced, so that short circuit between adjacent terminals is prevented.

These and other objects, advantages and features of the present invention will become more apparent from the following description and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1(a), 1(b) and 1(c) are cross sectional view showing the TFT array substrate for the liquid crystal display according to the present invention, and depicting fabrication steps of the TFT array substrate;

Fig. 2(a), 2(b) and 2(c) are cross sectional view showing the TFT array substrate for the liquid crystal display according to the present invention, and depicting fabrication steps of the TFT array substrate following the step of Fig. 1(c);

Fig. 3 (a) is an enlarged plain view of the source terminal on the TFT array substrate for the liquid crystal display according to the present invention, and Fig. 3(b) is a cross sectional view taken along line A-A in Fig. 3(a);

Fig. 4 is a schematic plan view showing a TFT array substrate

for liquid crystal display;

Fig. 5 is an enlarged plain view showing a TFT array substrate for liquid crystal display and depicting pixel electrodes, TFTs and source lines;

Fig. 6(a), 6(b) and 6(c) are cross sectional view showing a TFT array substrate for the conventional liquid crystal display, and depicting fabrication steps of the TFT array substrate;

Fig. 7(a), 7(b) and 7(c) are cross sectional view showing the TFT array substrate for the conventional liquid crystal display, and depicting fabrication steps of the TFT array substrate following the step of Fig. 6(c); and

Fig. 8 (a) is an enlarged plain view of a source terminal on the TFT array substrate for the conventional liquid crystal display, and Fig. 8(b) is a cross sectional view taken along line B-B in Fig. 8(a).

DETAILED DESCRIPTION

Hereinafter, embodiment of the present invention is described with referring to Figs. 1, 2 and 3.

Figs. 1 and 2 are cross sectional view of the TFT array substrate showing a TFT and a source terminal formed thereon, and describing fabrication steps thereof. Fig. 3 is a magnified view of the source terminal 18 in Fig. 2(c). Fig. 3(a) is a plain view of the source terminal 18, and Fig. 3(b) is a cross sectional view taken along line A-A in Fig. 3(a).

In the figure, a transparent insulating substrate 1, such as a glass substrate, is shown. Of course, a simply insulating substrate is also applicable. On the substrate 1, a gate line 2 and a supplementary

line 3 are formed. The supplementary line 3 is for connecting the terminal to the short-circuit ring 23. The gate line 2 and the supplementary line 3 are made from a metal film such as a film of Al or Cr. On the gate line 2 and the supplementary line 3, a gate insulating layer 4 covering the substrate 1 is formed. The gate insulating layer 4 is made of silicon nitride.

Above the gate line 2 and interposing the gate insulating layer 4, a semiconductor layer 5 is formed. The semiconductor layer 5 is made from, for example, a film of amorphous silicon. On the semiconductor layer 5, a contact layer 6 is formed. The contact layer 6 is made from a film of n+ amorphous silicon. On the contact layer 6, a source electrode 7 and a drain electrode 8 are formed. With the source electrode 7 and the drain electrode 8, a source line 9 is formed at the same time. By partly etching the contact layer 6, a channel is formed. Not to expose the TFT 17, a passivation film 11 is formed. The passivation film 11 is made of silicon nitride.

On the drain electrode 8 and through the passivation film 11, a contact hole 12 is formed for connecting the drain electrode 8 with a pixel electrode 15. On the source line 9 and through the passivation film 11, a contact hole 13 is formed for connecting the source line 9 with a terminal electrode 16. On the supplementary line 3 through the gate insulating layer 4 and the passivation film 11, a contact hole 14 is formed for connecting the supplementary line 3 with the terminal electrode 16. The pixel electrode 15 is made from a film of indium tin oxide (ITO). With the pixel electrode 15, the terminal electrode 16 is formed from the same ITO film at the same time.

Hereinafter, fabrication process of the TFT array substrate is

described more in detail with referring to Figs. 1, 2 and 3.

First of all, a metal film, such as a film of Cr or Al, is formed on an insulating substrate 1 by sputtering method. Then, the film is patterned using photo resist through photolithography to form a gate line 2 and a supplementary line 3 (Fig. 1(a)). To pattern the metal film, e.g. the film of Cr or Al, wet-etching method is used. Therefore, through investigation on the composition of the etchant, side surfaces of the gate and supplementary lines are taperingly etched, so that coverage of a layer formed thereon can be improved.

Thereafter, a silicon nitride film as a gate insulating layer 4 is deposited onto the substrate 1 with the gate line 2 and the supplementary line 3, by a plasma CVD method (Fig. 1(b)). Further, an amorphous silicon film is formed thereon, and successively, a n+ amorphous silicon film in which impurities are doped is formed. Then, the amorphous silicon film and the n+ amorphous silicon film are simultaneously patterned using photo resist through photolithography to form a semiconductor layer 5 and the contact layer 6 of TFT above the gate line 2 (Fig. 1(c)).

Afterwards, a metal film such as Cr film or Al film is formed by a method such as sputtering. Then, the film is patterned using photo resist through photolithography to form a source electrode 7, drain electrode 8 and source line 9. Thereafter, the n+ amorphous silicon (contact layer 6) is partly etched, that is, an area on which neither the source electrode 7 nor the drain electrode 8 is formed is etched through dry-etching process, so that the channel 10 is formed (Fig. 2(a)).

Then, to provide protection for TFTs, a silicon nitride film as a passivation film 11 is deposited by a method such as plasma CVD.

Thereafter, through dry-etching process using photo resist by photolithography, contact holes 12, 13 and 14 are formed (Fig. 7(b)). As described above, the contact hole 12 is for connecting the drain electrode 8 with a pixel electrode 15, the contact hole 13 is for connecting the source line 9 with a terminal electrode 16, and the contact hole 14 is for connecting the supplementary line 3 with a terminal electrode 16.

Afterwards, a transparent conductive film such as an ITO film is formed by a method such as sputtering. Then, the film is patterned using photo resist through photolithography, so that the pixel electrode 15 and the terminal electrode 16 are formed simultaneously.

As described, therefore, the source line 9 is connected to the supplementary line 3 via the contact hole 13, terminal electrode 16 and contact hole 14, and the supplementary line 3 is connected to the short circuit ring 23.

For the TFT array substrate thus fabricated, an alignment film is further formed. Then, a counter substrate, in which a black matrix, a counter electrode and an alignment film are formed on a transparent insulating substrate, is arranged facing to the TFT substrate. Liquid crystal is injected between the substrates and sealed with sealant. Thereafter, the edge of the TFT array substrate is cut off to remove the short-circuit ring 23 and the cut edge is chamfered off, thus the liquid crystal display is fabricated.

As is already described above and as shown in enlarged view in Fig. 3, two metallic lines below the terminal electrode 16 are made from different metallic layers, in the TFT substrate according to the present embodiment. Namely, in the display area side (the right side in Fig. 3), a metallic line below the terminal electrode 16 is the source line 9

which is made from the metal film for the source electrode 7 and the drain electrode 8. While, in the edge side of the substrate, that is, the short-circuit ring side (the left side in Fig. 3), a metallic line below the terminal electrode 16 is the supplementary line 3 which is made from the metal film for the gate line 2.

In the TFT substrate according to the present invention, the metallic line around the cutting line 24 in Fig. 3, that is, the supplementary line 3 is arranged under the gate insulating layer. Therefore, the supplementary line 3 is not scraped or only slightly scraped through the chamfering process, so that occurrence of the peeled metal pieces is minimized. Moreover, by the gate insulating layer 4 covering the supplementary line 3, peeling of the supplementary line 3 as well as generation of peeled metal pieces can be decreased, so that occurrence of short circuit between terminals is prevented.

In the embodiment described above, the TFT array substrate, in which the source electrode and the source line are formed in an upper layer than the gate line and short-circuit between source terminals is problematic, is explained. However, of course in the TFT array substrate where the gate line is formed in an upper layer than the source line, peeling of gate line at the cut and chamfered edge can be suppressed and short circuit between the gate lines can be prevented according to the present invention.

As described above, according to the present invention in which a metallic line at the short-circuit ring side and a metallic line at the display area side are in different layers below the terminal electrode of the terminal, peeling of the metallic line by cutting and chamfering process of the substrate can be suppressed. Therefore, occurrence of

peeled metal pieces can be reduced, so that short circuit between terminals is prevented to obtain a liquid crystal display of high reliability. Moreover, even in case where cutting and chamfering are performed proximately to the terminal electrode, short circuit between terminals is prevented. Therefore, requirement for high accuracy cutting and chamfering equipment, size of liquid crystal display and waste material due to cutting are reduced.

While preferred embodiment of the present invention has been described, such descriptions are for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the sprit or scope of the present invention.